Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **FB/SD**
2. **CAP+**
3. **GND**
4. **CAP-**
5. **VOUT**
6. **VREF**
7. **OSC**
8. **VCC**

**.120”**

**8**

**8**

**1**

**2**

**7**

**2**

**3**

**4**

**5**

**6**

**1054C**

**MASK**

**REF**

**.090”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref: 1054C**

**APPROVED BY: DK DIE SIZE .090” X .120” DATE: 9/6/23**

**MFG: TI / LINEAR TECH THICKNESS .020” P/N: LT1054**

**DG 10.1.2**

#### Rev B, 7/1